AF/2188

PTO/SB/21 (09-04)
Approved for use through 07/31/2006 OMB 0651-0031
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE


# TRANSMITTAL FORM

*(to be used for all correspondence after initial filing)*

Total Number of Pages in This Submission

| | |
|---|---|
| Application Number | 09/242,974 |
| Filing Date | February 26, 1999 |
| First Named Inventor | UGON, MICHEL |
| Art Unit | 2183 |
| Examiner Name | A. LI |
| Attorney Docket Number | T2146-906088 |

**ENCLOSURES** *(check all that apply)*

- [x] Fee Transmittal Form
  - [x] Fee Attached
- [ ] Amendment / Reply
  - [ ] After Final
  - [ ] Affidavits/declaration(s)
- [x] Extension of Time Request
- [ ] Express Abandonment Request
- [ ] Information Disclosure Statement
- [ ] Certified Copy of Priority Document(s)
- [ ] Reply to Missing Parts/ Incomplete Application
  - [ ] Reply to Missing Parts under 37 CFR 1.52 or 1.53
- [ ] Assignment Papers *(for an Application)*
- [ ] Drawing(s)
- [ ] Declaration and Power of Attorney
- [ ] Licensing-related Papers
- [ ] Petition
- [ ] Petition to Convert to a Provisional Application
- [ ] Power of Attorney, Revocation Change of Correspondence Address
- [ ] Terminal Disclaimer
- [ ] Request for Refund
- [ ] CD, Number of CD(s) ___
- [ ] After Allowance Communication to TC
- [ ] Appeal Communication to Board of Appeals and Interferences
- [ ] Appeal Communication to TC (Appeal Notice, Brief, Reply Brief)
- [ ] Proprietary Information
- [ ] Status Letter
- [ ] Application Data Sheet
- [ ] Issue Fee – Part B – Fee(s) Transmittal
- [x] Other Enclosure(s) (*please identify below*):

**Request for Reconsideration After Final**

Remarks

[x] The Commissioner is hereby authorized to charge any additional fees required or credit any overpayments to Deposit Account No. 50-1165 (T2146-906088) for the above identified docket number.

**SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT**

| | |
|---|---|
| Firm Name | Customer No. 000181 |
| Signature | |
| Printed Name | Jason H. Vick, Reg. No. 45,285 |
| Date | March 15, 2005 |

**CERTIFICATE OF MAILING OR TRANSMISSION**

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to: Mail Stop _____, Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450, or being facsimile transmitted to the USPTO at _____, on _____.

| | | | |
|---|---|---|---|
| Signature: | | | |
| Name: | | Date | |

PTO/SB/17 (12-04v2)
Approved for use through 07/31/2006. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE


Effective on 12/8/2004
Fees pursuant to the Consolidated Appropriations Act, 2005 (H.R. 4818)

# FEE TRANSMITTAL For FY 2005

*Patent fees are subject to annual revision.*

☐ Applicant claims small entity status. See 37 CFR 1.27

| TOTAL AMOUNT OF PAYMENT | $120.00 |
|---|---|

| *Complete if Known* | |
|---|---|
| Application Number | 09/242,974 |
| Filing Date | February 26, 1999 |
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| Examiner Name | A. LI |
| Art Unit | 2183 |
| Attorney Docket No. | T2146-906088 |



## METHOD OF PAYMENT *(check all that apply)*

☒ Check ☐ Credit Card ☐ Money Order ☐ None ☐ Other (please identify):_____

☐ Deposit Account Deposit Account Number: 50-1165 Deposit Account Name: Miles & Stockbridge P.C.

For the above-identified deposit account, the Director is hereby authorized to: (check all that apply)

☐ Charge fee(s) indicated below ☐ Charge fee(s) indicated below, **except for the filing fee**

☒ Charge any additional fee(s) or underpayments of fee(s) ☒ Credit any overpayments

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## FEE CALCULATION

### 1. BASIC FILING, SEARCH, AND EXAMINATION FEES

| | FILING FEES | | SEARCH FEES | | EXAMINATION FEES | | |
|---|---|---|---|---|---|---|---|
| | | Small Entity | | Small Entity | | Small Entity | |
| Application Type | Fee ($) | Fee ($) | Fee ($) | Fee ($) | Fee ($) | Fee ($) | Fees Paid ($) |
| Utility | 300 | 150 | 500 | 250 | 200 | 100 | |
| Design | 200 | 100 | 100 | 50 | 130 | 65 | |
| Plant | 200 | 100 | 300 | 150 | 160 | 80 | |
| Reissue | 300 | 150 | 500 | 250 | 600 | 300 | |
| Provisional | 200 | 100 | 0 | 0 | 0 | 0 | |

### 2. EXCESS CLAIM FEES

| Fee Description | Fee ($) | Small Entity Fee ($) |
|---|---|---|
| Each claim over 20 (including Reissues) | 50 | 25 |
| Each independent claim over 3 (including Reissues) | 200 | 100 |
| Multiple dependent claims | 360 | 180 |

| Total Claims | Extra Claims | Fee ($) | Fee Paid ($) |
|---|---|---|---|
| _____ - 20 or HP = | _____ | x _____ | = _____ |

HP = highest number of independent claims paid for, if greater than 20.

| Indep. Claims | Extra Claims | Fee ($) | Fee Paid ($) |
|---|---|---|---|
| _____ - 3 or HP = | _____ | x _____ | = _____ |

HP = highest number of independent claims paid for, if greater than 3.

| Multiple Dependent Claims | |
|---|---|
| Fee ($) | Fee Paid ($) |
| _____ | _____ |

### 3. APPLICATION SIZE FEE

If the specification and drawings exceed 100 sheets of paper (excluding electronically filed sequence or computer listings under 37 CFR 1.52(e)), the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).

| Total Sheets | Extra Sheets | Number of each additional 50 or fraction thereof | Fee ($) | Fee Paid ($) |
|---|---|---|---|---|
| _____ - 100 = | _____ / 50 = | _____ (round up to a whole number) x | _____ | = _____ |

### 4. OTHER FEE(S)

| | Fee Paid ($) |
|---|---|
| Non-English Specification, $130 fee (no small entity discount) | |
| Other (e.g., late filing surcharge): **Petition for Extension of Time** | $120.00 |

| SUBMITTED BY | | | | Complete *(if applicable)* | |
|---|---|---|---|---|---|
| Signature | | Registration No. *(Attorney/Agent)* | 45,285 | Telephone | (703) 903-9000 |
| Name *(Print/Type)* | Jason H. Vick | | | Date | March 15, 2005 |

Attorney Docket No. T2146-906088

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re Patent Application for:

First Named Inventor: UGON, MICHEL **Art Unit: 2183**

Appln. No.: 09/242,974 **Examiner: A. LI**

For: UNPREDICTABLE MICROPROCESSOR OR MICROCOMPUTER **Confirmation No.: 1762**

* * *

**REQUEST FOR RECONSIDERATION AFTER FINAL**

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In response to the outstanding Official Action mailed November 16, 2004, and in conjunction with the attached Petition for Extension of Time, Applicants respectfully request reconsideration of the above-identified application.

Claims 20-39 and 41-50 are pending with Claim 20 being independent. The Claims are rejected under various combinations of Okin, Fletcher and Griffin.

Independent Claim 20 is directed toward an unpredictable microprocessor or microcomputer. The unpredictable microprocessor or microcomputer includes a main memory, a first RAM-type working memory, a second RAM-type working memory, a processor, a bus and a switching means. The main memory includes an operating system, a main program, and a secondary program, wherein the secondary program is not related to the main program. The processor is adapted to execute instructions from one or more of said main memory, said first working memory and said second working memory. The bus connects the processor to the main memory, the first

working memory and the second working memory. The switching means makes the processor unpredictable, the switching means unpredictably jumping, while the programs are running, from one of the two working memories to the other working memory while saving the contents of the two working memories. (See Figure 1 of Applicant's Specification)

The switching means includes access registers associated with each of the main memory, the first working memory and the second working memory, at least one first block of registers stores the operating context of the programs in the main memory, and a switching circuit enables one of the working memories and controls the access registers associated with each of the main memory, the first working memory and the second working memory.

Applicants would initially like to point out that independent Claim 20 includes the structural features of a main memory. . . a first RAM-type working memory, a second RAM-type working memory, a processor . . . and a bus connecting the processor to the main memory, the first working memory, and the second working memory. Additionally, access registers are associated with each of the main memory, the first working memory and the second working memory.

Neither Okin, nor any of the other cited references, disclose a comparable structure. In contrast, and with reference to Figs. 3A and 3B (shown below with added highlights), Applicant believes Okin's processor 13 is connected to a cache memory and a main computer memory via local bus 28. The execution unit 14 of Okin, which is shown in greater detail in Fig. 3B, comprises the register files 32 and the other registers 38. Thus, in Okin, the cache memory and the main memory are outside the processor 13 but are connected thereto via local bus 28. There is absolutely no teaching or suggestion in Okin of the local bus 28, nor any other bus,

being able to connect the main memory, the first working memory, and the second working memory as claimed.

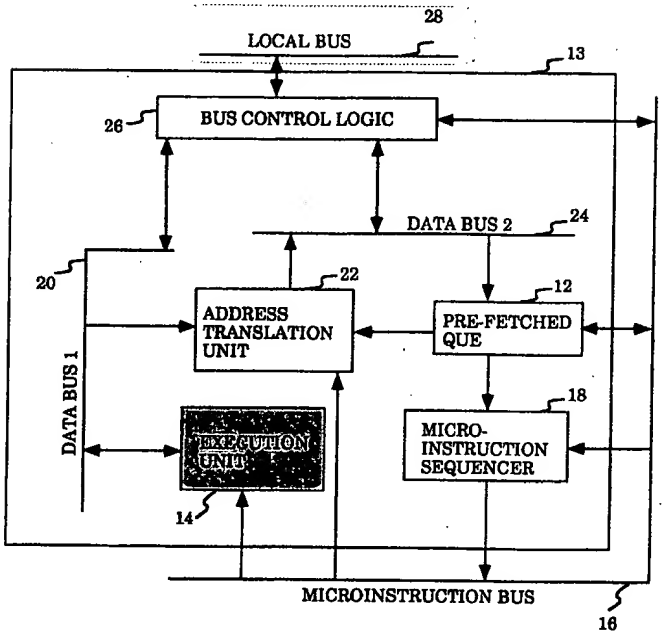


*FIGURE 3A*

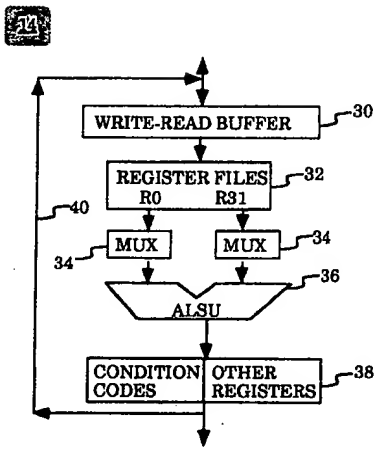


*FIGURE 3B*

The Office relies on Okin, column 1, lines 17-24; column 3, lines 62-64; and column 4, lines 6-26 for the teachings of the first RAM-type working memory and the second RAM-type memory as claimed. Based on these statements, Applicant is unsure as to which independent structural elements the Office is thereby relying on for each of the first and second claimed working memories as well as the claimed registers.

Regardless, the cache memory and main memory recited on column 1 of Okin, as well as the read-write buffer 30 and register file 32 mentioned on columns 3 and 4 of Okin, do not include the claimed structure of a bus connecting the processor to the main memory, the first working memory, and the second working memory. As discussed above, and in stark contrast, in Okin the register files 32 and other registers

38 are within the execution unit 14, and the main memory and cache memory are not only outside the execution unit 14, but are also outside processor 13 and connected to the local bus 28. There is not component(s) nor structure taught or suggested by Okin comparable to the claimed structure.

Moreover, Okin does not teach or suggest a processor adapted to execute instructions from one or more of said main memory, said first working memory and said second working memory, but only rather an arithmetic logic shift unit (ALSU) 36, which is part of the execution unit 14, which is itself a part of processor 13, that executes microinstructions. This is further evidenced by the other componentry in Okin, such as the micro-instruction sequencer 18 that is used for more complex instructions and is provided within the fast processor 13 (see, for example, column 3, lines 45-53 and Fig. 3A of Okin).

Accordingly, at least based on the above structural differences, Okin does not teach or suggest the configuration as claimed.

Additionally, Okin is directed toward switching the context of state elements of a very fast processor within a clock cycle when a cache miss occurs.... Okin is particularly useful for minimizing the average instruction cycle time for very fast processors with a main memory access time exceeding 15 processor clock cycles. Therefore, Okin is directed toward a pipelined processor with an objective of overcoming a completely different problem than the claimed invention that includes switching means for unpredictably jumping from one of the two working memories to the other working memory while saving the contents of the two working memories.

In Okin, the addressed problem is for reducing the penalty for cache misses and has absolutely nothing to do with an unpredictable microprocessor as claimed.

Okin is directed toward minimizing the penalty for cache misses and *maximizing* the speed of the processor by utilizing the pipeline to the fullest extent (see column 3, lines 31-34 of Okin). Fletcher is directed toward an operating system and, more particularly, to an operating system for multi-tasking operating environments. Fletcher absolutely does not teach or suggest the structural features nor the functionality as claimed. Moreover, Fletcher does not disclose the switching means that allows the processor to be unpredictable by unpredictably jumping from one of the two working memories to the other working memory as claimed. As with Okin, Fletcher is directed toward solving a completely different problem than the claimed invention and has nothing to do with enhancing security by using a first RAM-type working memory, a second RAM-type working memory and switching means as claimed.

Griffin is directed toward the determination of time of execution of a predetermined data processing routing in relation to the occurrence of prior externally observable events. As discussed on column 1 of Griffin, "the present invention generally pertains to data processing and is particularly directed to preventing compromise of secure data processing routines by a procedure known as a 'clock attack.'" In Griffin, the duration between the occurrence of the externally observable event and the execution of the predetermined routine is randomly varied. This "duration" is determined by the number of data processing clock cycles. Griffin is therefore directed toward solving a completely different problem from that of Okin, which is directed toward processing efficiency, and Fletcher, which is directed toward an operating system for a multi-tasking operating environment.

Furthermore, Applicants are concerned that the teachings from these two references may not be combinable in that in Okin, increasing processing efficiency is

the objective, while in Griffin, randomly varying the duration of the interim routines slows down processing.

In Griffin there is absolutely no teaching or suggestion of unpredictably jumping from one of the two working memories to the other working memory while saving contents of the two working memories as claimed. In stark contrast, Griffin is directed toward inhibiting synchronization with externally generated instructions by preventing determination of the time of execution of predetermined data processing routines in relation to the occurrence of an externally observable event that precedes the execution of the predetermined routine. The teaching of randomly varying the duration between the occurrence of the externally observable event and the execution of the predetermined routine does not anticipate or render obvious the claimed unpredictable microprocessor having a switching means that unpredictably jumps from one of the two working memories to the other working memory as claimed.

For this feature, the Office points to Griffin, columns 1-2, lines 58-11 and asserts "Griffin describes executing one or more interim data processing routines at random intervals. In order to execute these routines, the processor must jump from the current instruction address to the beginning address of the routine. By randomly varying the time intervals between these jumps and executing the current process, the device is unpredictable, since the definition of random, in relation to computing, is unpredictable. Please see the attached definition for more information."

In contrast to the Office's assertions, the claimed switching means that unpredictably jumps while the programs are running, from one of the two working memories to the other working memory, is a specific claimed technical feature that is entirely different than the asserted "randomly varying the time intervals between these jumps" as stated in Griffin.

There is absolutely no teaching or suggestion in Griffin, nor any of the cited references, of switching from one of the two working memories to the other working memory as claimed.

In contrast, Griffin teaches randomly varying the duration of interim routines in an effort to prevent a clock attack. In particular, Griffin states bridging columns 1 and 2 that:

> In one aspect of the present invention, step (a) includes the steps of (b) executing one or more interim data processing routines between the occurrence of the observable external event and the execution of the predetermined routine; and (c) randomly varying the duration of said interim routines. In this aspect of the invention, steps (b) and (c) preferably include the step of (d) randomly assembling m said interim routines for said execution from a group of n stored routines having different durations, wherein m and n are integers, with n being greater than m. It is also preferred that step (d) either includes the step of (e) randomly accessing said m interim routines from a secure memory; or the steps of (f) randomly accessing pointers for said m interim routines from a secure memory; and (g) accessing said m interim routines from a memory in response to said pointers.
>
> In a further aspect of the present invention, step (a) includes the steps of (b) executing one or more interim data processing routines between an occurrence of the externally observable event and the execution of the predetermined routine, wherein said interim routines includes a data processing routine that is essential to the execution of said overall larger data processing routine; and (c) randomly varying the duration of said interim routines.

Furthermore, Column 3, lines 27-36 of Griffin states:

> In order to prevent a predetermined protected routine ROUTINE N from being synchronized with the externally observable event that repetitively precedes the protected routine ROUTINE N, the BRANCH routine 12 causes

the CPU 10 to branch to the maze of m interim routines INTERIM ROUTINE 1, INTERIM ROUTINE 2, . . . , INTERIM ROUTINE m. The total duration of the m interim routines is a random variable. The m interim routines have different durations.

Column 6, lines 55-61 of Griffin states:

The n interim routines have different durations; and the selection and sequence of the m interim routines that are assembled for execution during a given data processing sequence is randomly varied from one sequence to the next in order to make the total duration of the interim routines a random variable. The values of the different durations of the interim routines are so distributed that a large number of the n.sup.m possible mazes of interim routines have a different total duration.

Column 7 of Griffin recites that:

The pointers 67, 68, 69 are fixed but the selection and sequence of the m pointers that are accessed during a given data processing sequence is randomly varied from one overall data processing cycle to the next in order to make the total duration of the interim routines a random variable. The selection and sequence of the m pointers is provided during each overall data processing cycle in response to a signal produced by a physically (truly) random phenomena, such as a noisy diode, or in response to a pseudorandom device, such as a pseudorandom number generator. ...

FIG. 5 illustrates an alternative preferred, embodiment of an interim routine. In this interim routine the duration between the externally observable event and the predetermined protected routine is randomly varied in response to both dynamically processed data that does not repetitively recur at the same time in

relation to each occurrence of the externally observable event, and data stored in a secure memory.

At least based on these passages, and Applicant's understanding of Griffin, there is simply no teaching or suggestion of unpredictably jumping from one of the two working memories to the other working memory while saving the contents of the two working memories as claimed. In contrast, Griffin is directed toward inhibiting synchronization with externally generated instructions by preventing determination of the time of execution predetermined data processing routine in relation to the occurrence of an externally observable event that precedes the execution of the predetermined routine. This is implemented by randomly varying the duration between the occurrence of the externally observable event and the execution of the predetermined routine (see Abstract).

At least based on the above, Applicants respectfully yet steadfastly maintain that the cited references, taken either alone or in combination, do not teach or suggest the features as recited in independent Claim 20. Moreover, Applicants respectfully submit that the motivation provided to combine the teachings of the references is untenable, in that the references teach away from each other's objectives and combinability. Furthermore, it is well established law that the mere fact that parts of prior art disclosures could in theory be combined does not make the combination obvious unless the prior art also contains something to suggest the desirability of the combination. To imbue one of ordinary skill in the art with knowledge of the invention, when no prior references of record convey or suggest that knowledge, is to fall victim to the insidious effect of hindsight syndrome where that which only the inventor taught is used against its teacher.

Accordingly, the rejection of Claim 20 is untenable and should be withdrawn. The claims that depend therefrom are also allowable over the references of record for at least the above reasons as well as the additional feature(s) recited therein. In that the outstanding rejection is untenable, a prompt Notice of Allowance is respectfully requested.

The Commissioner is hereby authorized to charge to deposit account number 50-1165 (T2146-906088) any fees under 37 CFR § 1.16 and 1.17 that may be required by this paper and to credit any overpayment to that Account. If any extension of time is required in connection with the filing of this paper and has not been separately requested, such extension is hereby requested.

Respectfully submitted,

By:_____
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March 14, 2005